

DLD Couse Assignment#4

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Section:   
CS-D

**Q-1**

**16x1 Multiplexer Circuit:**



**4x16 Decoder internal Circuit:**



**Q-2**

12x1 **Multiplexer Circuit**:

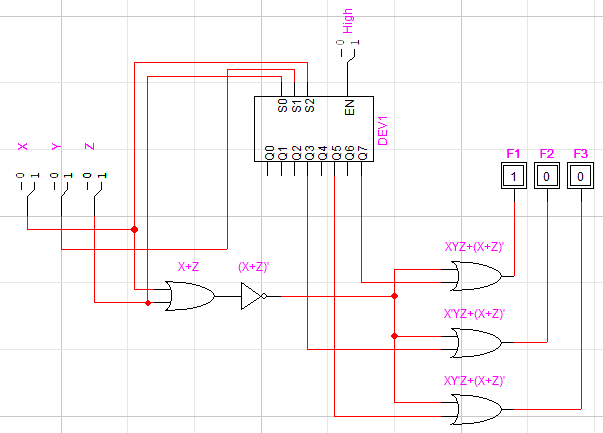


**Q-3**

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**Q-4**

Circuit:



TRUTH TABLE:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| X | Y | Z | X+Z | (X+Z)' | F1 | F2 | F3 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

**Q-5**

**(A)**

**Logic Diagram:**

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**Equations:**

**Before assumption:-**

LR=(BL.LT)+(BL.EM)+BR

RR=(BL.RT)+(BL.EM)+BR

**Before assumption:-**

LR=(BL.LT)

RR=(BL.RT)

**(B)**

**LR (BL, BR, EM, LT):**

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**Equation:**

LR=BLLTBREM+BLLTBREM'+BLLTBR'EM+BLLTBR'EM'+BLLT'BREM+BLLT'BR'EM+BLLT'BREM'+BL'LTBREM+BL'LT'BREM+ BL' LT BREM'+ BL' LT'BREM'

**RR (BL, BR, EM, RT):**



**Equation:**

RR=BLRTBREM+BLRTBREM'+BLRTBR'EM+BLRTBR'EM'+BLRT'BREM+BLRT'BR'EM+BLRT'BREM'+BL'RTBREM+BL'RT'BREM+ BL' RT BREM'+ BL' RT'BREM'

**Q-6**

**Logic Diagram:**

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F=AB + A'B'D + B'CD + BC'D'

F=ABCD+ABCD'+ABC'D+ABC'D' + A'B'CD+A'B'C'D + AB'CD +A'B'CD+ ABC'D'+A'BC'D'

F=AB(CD+CD'+C'D+C'D')+ A'B'(CD+C'D) + AB'CD+A'BC'D'

**Results:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | F=AB + A'B'D + B'CD + BC'D' | | |
| 0 | 0 | 0 | 0 | 0 |  |  |
| 0 | 0 | 0 | 1 | 1 |  |  |
| 0 | 0 | 1 | 0 | 0 |  |  |
| 0 | 0 | 1 | 1 | 1 |  |  |
| 0 | 1 | 0 | 0 | 1 |  |  |
| 0 | 1 | 0 | 1 | 0 |  |  |
| 0 | 1 | 1 | 0 | 0 |  |  |
| 0 | 1 | 1 | 1 | 0 |  |  |
| 1 | 0 | 0 | 0 | 0 |  |  |
| 1 | 0 | 0 | 1 | 0 |  |  |
| 1 | 0 | 1 | 0 | 0 |  |  |
| 1 | 0 | 1 | 1 | 1 |  |  |
| 1 | 1 | 0 | 0 | 1 |  |  |
| 1 | 1 | 0 | 1 | 1 |  |  |
| 1 | 1 | 1 | 0 | 1 |  |  |
| 1 | 1 | 1 | 1 | 1 |  |  |

**Q-7**

**Logic Diagram:**



**8 bit adder:**

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**Results:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S | A | B | Carry | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
| 1 | 11010 | 10001 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 11110 | 1110 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1111110 | 1111110 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 101001 | 101 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |

**Q-8**

**Logic Diagram:**



**Results:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S | A | B | Overflow | S5 | S4 | S3 | S2 | S1 | S0 |
| 0 | 100111 | 111001 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 001011 | 100110 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 110001 | 010010 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 101110 | 110111 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |

**Q-9**

**Logic Diagram:**

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**4 bit adder:**

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**Results:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| S | A | B | C4 | S3 | S2 | S1 | S0 |
| 0 | 0111 | 0111 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0100 | 0111 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1101 | 1010 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0111 | 1010 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0001 | 1000 | 0 | 1 | 0 | 0 | 1 |

**Q-10**

**Demultiplexer using 4x16 Decoder:**

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**Q-11**

**2 bit magnitude comparator:**

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**1 bit magnitude comparator:**

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TRUTH TABLE:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| a1 | a0 | b1 | b0 | L | E | G |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

**Q-12**

**Logic Diagram:**

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**4 bit adder:**

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**4 bit comparator:**

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**4 bit passer:**

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**Q-13**

**Logic Diagram:**

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**4 bit multiplier:**

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**8 bit adder:**

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**8 bit comparator:**

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**8 bit passer:**

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**THANK YOU**

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